DIGITAL LOGIC DESIGN

Course Code	19EC3401	**Year**	II	**Semester**	II
Course Category	Program Core	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Nil
Continuous Internal Evaluation	30	**Semester End Evaluation**	70	**Total Marks**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Compare the various features of Binary codes.
CO2	Simplify Boolean functions using K-map & implement them using Logic gates
CO3	Design and Realize various Combinational circuits for the given specifications
CO4	Analyze and Design Clocked Sequential circuits
CO5	Construct Logic gates using CMOS

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3-High, 2: Medium, 1:Low)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	2							1	2	1
CO2	3	3	2	2	2							1	2	1
CO3	3	3	2	2	2							1	2	1
CO4	3	3	2	2	3							1	2	1
CO5	3	3	2	2	3							1	2	1

Syllabus

Unit No.	Contents	Mapped CO
I	**BinaryCodes**: Signed Binary Numbers, Complements, Binary Codes, Error detection and correction code, Binary Logic. **Boolean Algebra**: Basic definitions, Axiomatic definition of Boolean algebra, Basic theorems and properties of Boolean algebra, Boolean functions, Canonical and standard forms,Digital logic gates.	CO1
II	**Simplification of Boolean functions**: The map method, Four-variable map, Five-variable map, Tabulation Method, Product of sums simplification, Don’t-care conditions, NAND and NOR implementation, Exclusive-or function. .	CO2
III	**Combinational Logic**: Combinational circuits, Analysis procedure, Design procedure, Binary Adder- Subtractor, Decoders, Encoders, Multiplexers, De-Multiplexer **Memories**: Random-access memory, Memory decoding, Read-only memory**.**	**CO3**
IV	**Synchronous Sequential Logic**: Sequential circuits, Latches, Flip-Flops, Analysis of clocked sequential circuits, State reduction and assignment, Design procedure	CO4
V	**Registers and Counters**: Registers, Shift registers, Ripple counters, Synchronous Counters, Ring counter. **Digital**	CO5

	Integrated circuits: Special characteristics, Complementary MOS (CMOS), CMOS transmission gate circuits.	

Learning Resources
Text Books
1. Michael D. Ciletti, M. Morris Mano, Digital Design, 4/e. Pearson Education, 2007.
Reference Books
1. ZviKohavi, Switching and Finite Automata Theory, 2/e, Tata McGraw-Hill Education, 2008. 2. John F. Wakerly, Digital Design Principles and Practices, 4/e, Pearson Education, 2008. 3. Frederick J. Hill and Gerald R. Peterson, Introduction to Switching Theory and Logic Design, 3/e, John Willey and Sons, 1981. 4. Charles Roth, Jr., Larry Kinney, Fundamentals of Logic Design, 7/e, Cengage Learning, India, 2013.
e- Resources & other digital material
1. http://www.ece.ubc.ca/~saifz/eece256.html 2. http://nptel.iitm.ac.in/courses/Webcourse-contents/IIT%20Guwahati/digital_circuit/frame/index.html

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